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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,898	09/24/2003	Cyril Cabral JR.	YOR920030469US1	2246

7590 06/29/2006

Moser, Patterson & Sheridan
Suite 100
595 Shrewsbury Avenue
Shrewsbury, NJ 07702

EXAMINER

SMITH, BRADLEY

ART UNIT	PAPER NUMBER
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2891

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/669,898	Applicant(s) CABRAL ET AL.	
	Examiner Bradley K. Smith	Art Unit 2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 April 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>4/3/06</u> | 6) <input checked="" type="checkbox"/> Other: <u>search notes</u> |

DETAILED ACTION

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim1 – 3, 5, 6, 9, 10, and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Maszara *et al.* (US 6,599,831) in view of Hizawa (US 2003/0096491).

Maszara *et al.* (US 6,599,831) discloses a method of fabricating a transistor **30** by providing a substrate **32**, providing a polysilicon layer **36** formed on a gate dielectric **34**, doping **50** the polysilicon layer, forming a polysilicon gate electrode [Figures 7 & 8], depositing a metal layer **60**, siliciding the gate electrode to form a silicide **62** and a monolayer **68** of the dopant at an interface between the gate dielectric and the silicide.

Regarding claim 2, Maszara *et al.* further discloses doping after the forming step [Figure 2].

Regarding claims 3, 5, and 6, Maszara *et al.* further discloses doping with As or B with an ion implantation process with a dose of 1×10^{14} to 4×10^{15} ions/cm² [column 3, lines 10-20].

Regarding claims 9 and 10, Maszara *et al.* further discloses using Ni [column 3, line 45].

Regarding claim 13, Maszara *et al.* further discloses siliciding using an annealing process [column 3, lines 30-35].

However Masazara fails to disclose having an elevated source and drain, whereas Hizawa disclose the use of an elevated source and drain/ SOI structure (see figure14).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Masazara and Hizawa because the SOI structure would have lower power consumption and lower resistance (see paragraph 0009).

Claim 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Masazara and Hizawa as applied to claim 1 above, and further in view of Buynoski.

Regarding claim 4, Maszara *et al.* and Hizawa teach using B or As as a dopant, but not Sb. Buynoski (US 6,518,113) teaches B, As, P, or Sb as a dopant [column 12, lines 1-10]. It would have been obvious to one of ordinary skill in the art to use Sb as a dopant since Buynoski teaches that Sb is an equivalent material choice and therefore is well known as a substitute for B or As.

Claims 7, 8, 11, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masazara and Hizawa as applied to claim 1 above, and further in view of Chong *et al.*

Regarding claims 7 and 8, Maszara *et al.* and Hizawa do not discuss amorphizing the gate electrode. Chong *et al.* (6,624,489) teaches amorphizing the

polysilicon gate electrode by ion implanting Si or Ge [column 4, lines 50-60]. It would have been obvious to one of ordinary skill in the art to amorphize the gate electrode since Chong *et al.* teaches that this process breaks the lattice bonds of the silicon surface and reduces the temperature needed for annealing.

Regarding claims 11 – 12, Maszara *et al.* and Hizawa teach Ni, but does not discuss Co or an alloy of Ni. Chong *et al.* teaches a metal of Ni or Co and an alloy of Pt [column 4, line 65]. It would have been obvious to one of ordinary skill in the art to use the materials of Chong *et al.* in the method of Maszara *et al.* since Chong *et al.* teaches that Co or Ni-Pt is well known material choice for forming silicide layers with the same properties and function as Ni.

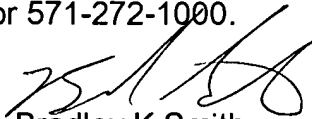
Regarding claim 14, Maszara *et al.* and Hizawa further teaches a rapid thermal annealing process performed at 500° C, but does not discuss the annealing time. Chong *et al.* teaches a siliciding process of annealing between 250° C and 900° C for 5 sec to 1 hr [column 6, lines 22-23]. It would have been obvious to one of ordinary skill in the art to use an annealing time of 0.3 to 30 min in the process of Maszara *et al.* since Chong *et al.* teaches that this annealing time is sufficient to use all of the metal layer which is necessary to the Maszara *et al.* process [column 4, lines 25-35].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley K. Smith whose telephone number is 571-272-1884. The examiner can normally be reached on 10-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Bradley K Smith
Primary Examiner
Art Unit 2891